

AMC524 / AMC524C – Quad ADC, 16-bit @ 125 MSPS, Dual DAC, Artix-7

Quad ADC, Dual DAC, Artix-7



AMC524C

KEY FEATURES

- Quad ADC 16-bit @ 125 MSPS (AD9653)
- Dual DAC 12-bit @ 2.5 GSPS (DDS AD9915)
- Artix-7 FPGA with dual banks of DDR-3, 2 GB total
- Conduction cooled version available
- Internal, external or backplane clock with on-board wide-band PLL
- AMC Ports 4-7 and 8-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (PCIe, SRIO, XAUI, etc. are FPGA programmable)
- Single module, mid-size per AMC.0
- IPMI 2.0 compliant

AdvancedMC™

Benefits of Choosing VadaTech

- Calibration-free stable dynamic performance at all temperatures
- BSP support and example code
- Strong mil/aero support
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

The AMC524 provides a Direct Digital Synthesizer (DDS) capable of generating a frequency-agile analog sinusoidal waveform (up to 1.0 GHz). The chipset includes a PLL for clock cleaning, along with a versatile internal timing and control mechanism. The unit supports fast frequency hopping and a linear sweep mode of frequency, phase or amplitude.

The AMC ports 0-15 are all routed to the FPGA from the AMC connector, providing the user with flexibility to support standard base and fabric interface or custom high-bandwidth interconnects (depending on backplane capabilities). The FPGA is supported by 1 GB FLASH memory for boot image storage and dual banks of DDR3 for local data storage.

TCLK A-D and FCLK are routed to the FPGA via an on-board clock and jitter cleaner. The module supports internal or external clocking. The modules allows for RF Clock synthesis for the DAC and the ADC to come from the front panel or from the on-board wideband PLL.

The AMC524 is available in both air-cooled (MTCA.0 and MTCA.1) and rugged conduction-cooled (MTCA.2 or MTCA.3) versions.

REFERECE DESIGN

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is geared to prove out the hardware for engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application.

AMC524

BLOCK DIAGRAM

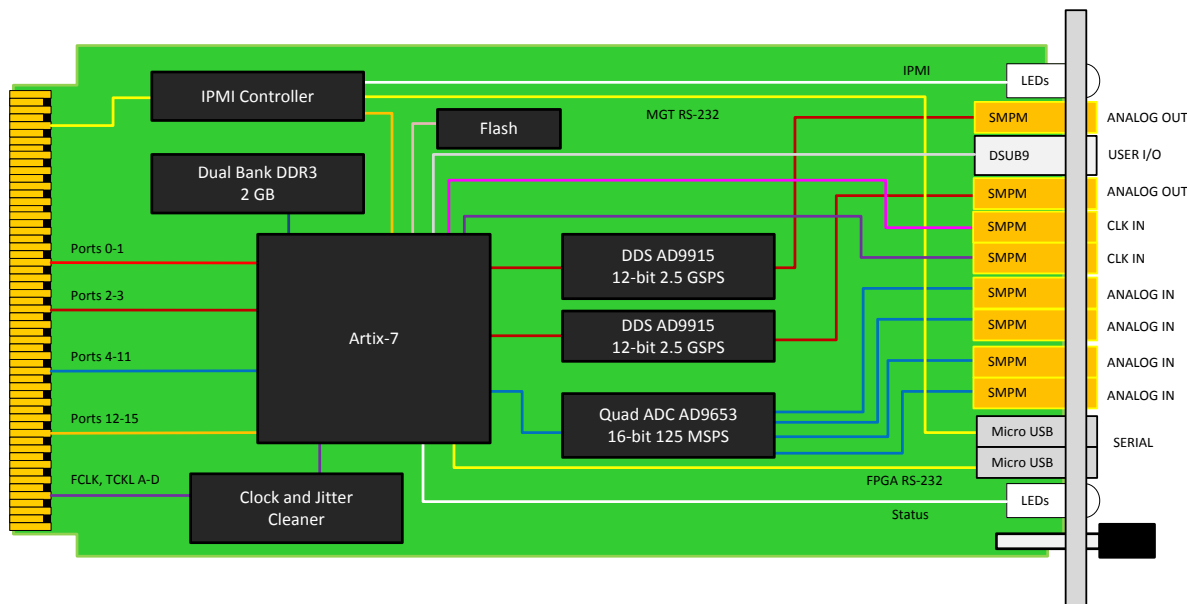


Figure 1: Functional Block Diagram

FRONT PANEL

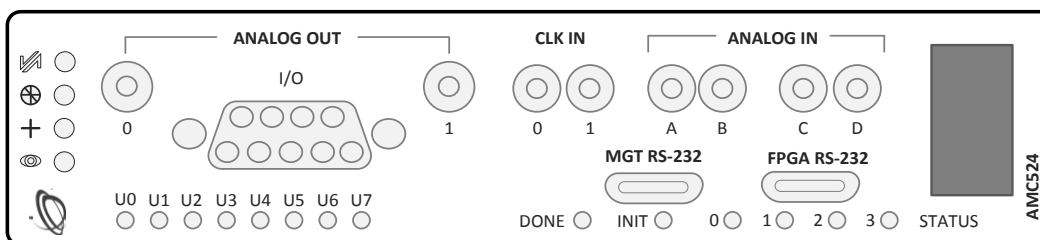


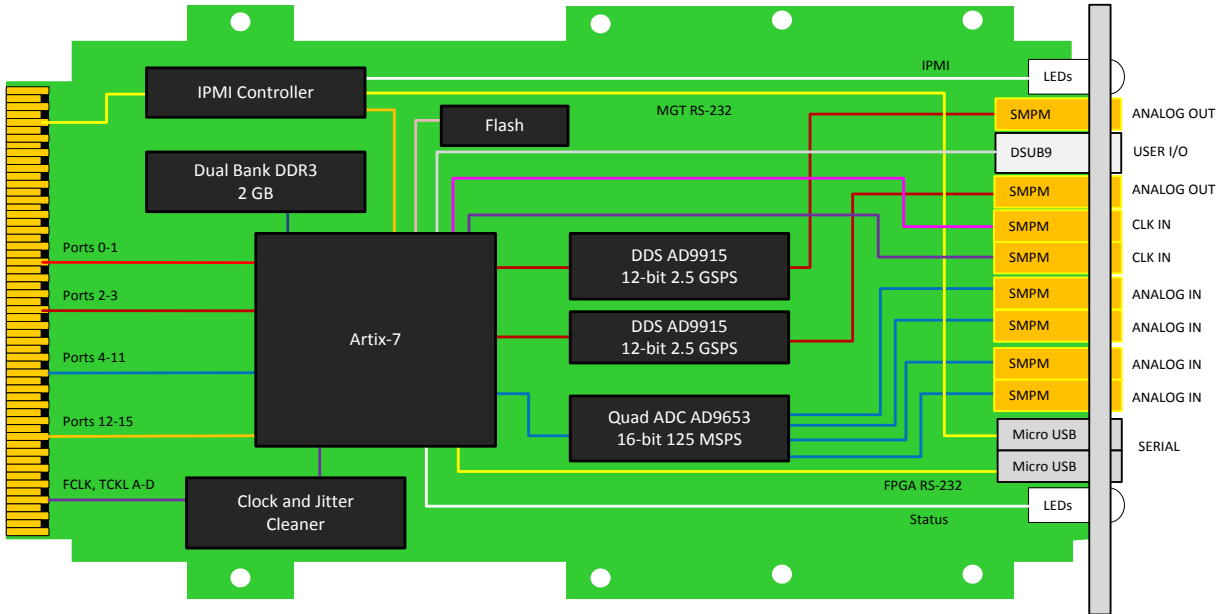
Figure 2: AMC524 Front Panel

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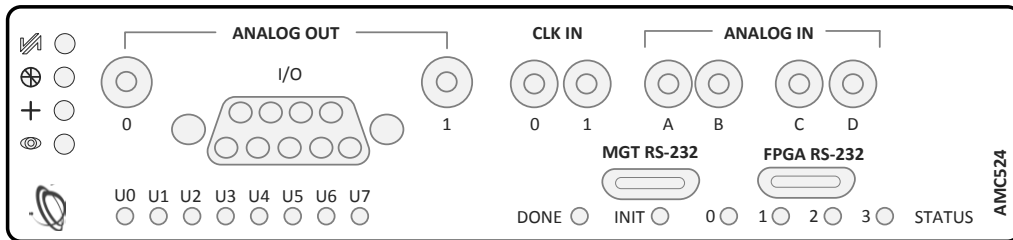
AMC524C

VadaTech offers the AMC524 in a rugged clamshell variant, available as either MTCA.3 (conduction cooled) or MTCA.2 (hybrid cooled, forced air and conduction). For these versions of the module the ground planes are extended into the wedge lock region of the clamshell to enhance thermal transfer, as shown below. Such units are typically used in ATR style chassis such as the VT87x series.

BLOCK DIAGRAM



FRONT PANEL



SPECIFICATIONS

Architecture		
Physical	Dimensions	Single module, mid-size (full-size optional)
		Width 2.89" (73.5 mm) Depth 7.11" (180.6 mm)
Type	AMC ADC	Quad ADC with Artix-7 FPGA (XC7A200T)
		16-bit resolution per port on ADC Internal/External clock with TRIG IN/OUT
Standards		
AMC	Type	AMC.0, AMC.1, AMC.2, AMC.4 (FPGA programmable)
Module Management	IPMI	IPMI Version 2.0
PCIe	Lanes	Dual x4 via FPGA to AMC
SRIO	Lanes	Dual x4 via FPGA to AMC
XAUI	Lanes	Dual port XAUI
Ethernet	Lanes	Dual GbE per AMC.1
Configuration		
Power	AMC524	15 W (Application Specific)
Environmental	Temperature	Operating temperature: -5° to 45° C (55°C for limited time, performance restrictions may apply), industrial and military versions also available (See environmental spec sheet)
		Storage Temperature: -40° to +85°C
	Vibration	1G, 5 to 500 Hz on each axis
	Shock	30Gs each axis
Front Panel	Interface Connectors	FPGA JTAG port via a flex cable
		4 ADC and 2 DAC via SMPM connector
		FPGA and IPMI RS-232 via Micro USB
	LEDs	Trigger I/O via SMPM
		IPMI Management Eight user defined LEDs
Mechanical	Hot Swap Ejector Handle	
Software Support	Operating Systems	Independent
Other		
MTBF	MIL Hand book 217-F @ TBD Hrs	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and μ TCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information

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ORDERING OPTIONS

AMC524 – ABC – DEF – G0J

A = DAC RF Clock Synthesis

- 0 = Front panel
- 1 = On Board wide band PLL

B = ADC RF Clock Synthesis

- 0 = Front panel
- 1 = On Board wide band PLL

C = Front Panel

- 1 = Reserved
- 2 = Mid-size
- 3 = Full-size
- 4 = Reserved
- 5 = Mid-size, MTCA.1 (captive screw)
- 6 = Full-size, MTCA.1 (captive screw)

D = FPGA

- 0 = XC7A200T
- 1 = Reserved
- 2 = Reserved

E = FPGA Speed

- 0 = Reserved
- 1 = High
- 2 = Highest

F = PCIe Option

- 0 = None
- 1 = PCIe on Ports 4-7
- 2 = PCIe on Ports 8-11
- 3 = PCIe on Ports 4-11

G = Ports 12-15

- 0 = Routed to FPGA
- 1 = Not Routed to FPGA

J = Temperature Range and Coating

- 0 = Commercial (–5° to +55° C), No coating
- 1 = Commercial (–5° to +55° C), Humiseal 1A33 Polyurethane
- 2 = Commercial (–5° to +55° C), Humiseal 1B31 Acrylic
- 3 = Industrial (–20° to +70° C), No coating
- 4 = Industrial (–20° to +70° C), Humiseal 1A33 Polyurethane
- 5 = Industrial (–20° to +70° C), Humiseal 1B31 Acrylic
- 6 = Military (–40° to +85° C), Humiseal 1A33 Polyurethane*
- 7 = Military (–40° to +85° C), Humiseal 1B31 Acrylic*

AMC524C – ABC – DEF – G0J

A = DAC RF Clock Synthesis

- 0 = Front panel
- 1 = On Board wide band PLL

B = ADC RF Clock Synthesis

- 0 = Front panel
- 1 = On Board wide band PLL

C = Ruggedization Level*

- 0 = None
- 1 = Contact Vadatech
- 2 = Contact Vadatech
- 3 = Contact Vadatech

D = FPGA

- 0 = XC7A200T
- 1 = Reserved
- 2 = Reserved

E = FPGA Speed

- 0 = Reserved
- 1 = High
- 2 = Highest

F = PCIe Option

- 0 = None
- 1 = PCIe on Ports 4-7
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* Ruggedization level is per the uTCA.2 and uTCA.3 specification

** Edge of module

RELATED PRODUCTS



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Development Chassis 8 Slots



UTC004 3rd Gen MCH for
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