

AMC538

Altera Carrier for FMC, Stratix-10™

Key Features

- Altera Stratix-10 (Option for GX1650 or GX2800)
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4
- AMC Ports 12-15 and 17-20 are routed to the FPGA
- Single module, mid-size AMC (full-size optional)
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- Clock jitter cleaner
- 16 GB of DDR-4 (dual bank of 64-bits)

Benefits

- Stratix-10 FPGA
- Dual Bank of 64-bit wide DDR4 memory allows larger buffer sizes while processing and queuing data to the host
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

AdvancedMC™



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AMC538

The AMC538 is based on the Altera Stratix-10™ GX1650/2800 FPGA. It is compliant to AMC.1, AMC.2, AMC.3 and/or AMC.4 specifications.

The module routes all LA/HA/HB and 10 DP SERDES to the FMC slot. The on-board, re-configurable FPGA interfaces directly to the AMC FCLKA and TCLKA–D via a Cross Bar Switch (CBS) MLVDS.

The FPGA has two banks of DDR4, 64-bit wide, with 16 GB total memory. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

Block Diagram

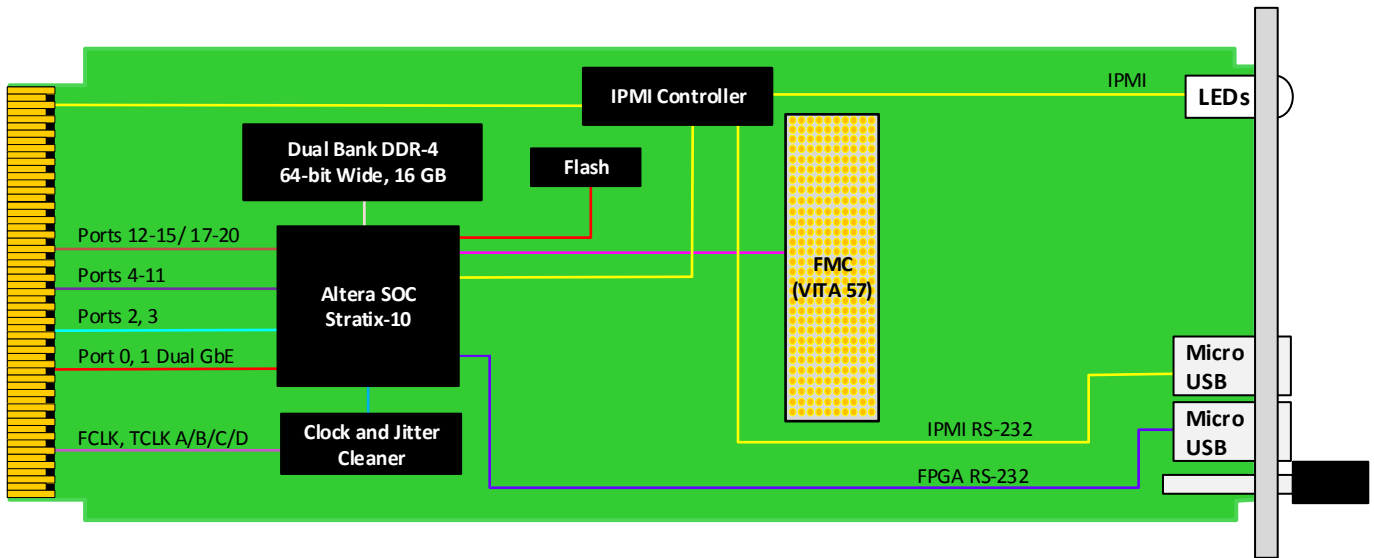


Figure 1: AMC538 Functional Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

Specifications

Architecture		
Physical	Dimensions	Single module, mid-size (full-size optional) Width: 2.89" (73.5 mm) Depth 7.11" (180.6 mm)
Type	AMC FPGA	Stratix-10™ FPGA
Memory		Dual bank of DDR4 (64-bit wide)
Standards		
AMC	Type	AMC.0, AMC.1, AMC.2, AMC.3 and/or AMC.4
Module Management	IPMI	IPMI v2.0
PCIe	Lanes	Dual x4 or single x8 via FPGA to AMC
SRIO	Lanes	Dual x4 via FPGA to AMC
Ethernet	1/10/40G	Dual 1/10/40 GbE via FPGA (ports 0-1 and 4-11)
Configuration		
Power	AMC538	~40 W (application specific)
Environmental	Temperature	See ordering options and environmental spec sheet Storage Temperature: -40° to +85°C
	Vibration	Operating 9.8 m/s ² (1 G), 5 to 500 Hz on each axis
	Shock	30 G each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	Interface Connectors	Dual micro USB for MGT RS-232 and FPGA RS-232 Single FMC slot
	LEDs	IPMI management control Four user defined LEDs
	Mechanical	Hot swap ejector handle
Software Support	Operating System	Linux
Other		
MTBF		MIL Hand book 217-F@ TBD hrs
Certifications		Designed to meet FCC, CE and UL certifications, where applicable
Standards		VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards
Warranty		Two (2) years

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC538 – A0C-DEF-G0J

A = Ports 12-15/17-20	D = FPGA	G = Clock Holdover Stability
0 = Not routed to FPGA 1 = Routed to FPGA	0 = GX1650 1 = GX2800 2 = Reserved 3 = Reserved	0 = Standard XO 1 = Stratum-3 (TCXO)
	E = FPGA Speed	
	1 = Highest 2 = High 3 = Reserved	
C = Front Panel Size	F = PCIe Option	J = Temperature Range and Coating
1 = Reserved 2 = Mid-size (4HP) 3 = Full-size (6HP) 5 = Mid-size, MTCA.1 (captive screw) 6 = Full-size, MTCA.1 (captive screw)	0 = No PCIe 1 = PCIe on ports 4 – 7 2 = PCIe on ports 8 – 11 3 = PCIe on ports 4 – 11	0 = Commercial (–5° to +55° C), No coating 1 = Commercial (–5° to +55° C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55° C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70° C), No coating 4 = Industrial (–20° to +70° C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70° C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85° C), Humiseal 1A33 Polyurethane* 7 = Extended (–40° to +85° C), Humiseal 1B31 Acrylic*

Notes: *Conduction cooled, temperature is at edge of module. Consult factory for availability

Related Products

AMC532



- AMC FPGA based on Altera Stratix-V (5SGXEA) in F1932 package
- VITA 57.1 FMC HPC Connector (compatible with LPC)
- All FMC LA, HA, HB pairs routed bi-directionally

FMC227



- Dual AD9625 ADC
- Wide full power bandwidth supports IF sampling of signals up to 2 GHz
- Single DAC AD9129

UTC004



- Unified 1GHz quad-core CPU for MCMC (MicroTCA Carrier Management Controller), Shelf Manager, Clocking, and Fabric management
- Automatic fail-over with redundant UTC004s
- 1GbE base switch with dual 100/1000/10G uplink

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