# AMC573

## Zynq UltraScale+ RFSoC FPGA, AMC

## Key Features

- Xilinx UltraScale+ RFSoC XCZU28DR FPGA
- 8 ADC/DAC to the front
- 8 GB of 64-bit wide DDR-4 Memory (single bank) with ECC to CPU
- 8 GB of 64-bit wide DDR-4 Memory (single bank to Fabric)
- MPSoC with block RAM and UltraRAM
- SD Card (option)
- 128 MB of boot Flash
- 64 GB of user Flash

## Benefits

- High density I/O all to front panel
- Zynq UltraScale+ MPSoC+ RF
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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# AMC573

The AMC573 utilizes the Xilinx XCZU28DR RFSoC. The AMC is compliant to AMC.1, AMC.2, AMC.3 and AMC.4 specifications. The unit has an on-board, re-configurable FPGA which interfaces directly to the AMC FCLKA, TCLKA-D. The module has dual bank of 64-bit wide DDR-4 memory with ECC for a total of 16 GB. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The front panel has 18 high density RF Coaxial style connectors which brings into the RFSoC the 8 ADC (12-bit at 4 GSPS) and 8 DAC (14-bit at 6.4 GSPS). In addition, there are Trig-in Trig-out as well as clock inputs via the front panel. The front panel also has the interface to the DisplayPort, dual USB, RS-232 ports as well as dual high-density connector for external I/O (RS-422 and single ended 3.3 V).

The XCZU28DR includes a quad-core ARM Cortex-A53 application processing unit and dual-core Cortex-R5 real-time processing as well as over 4,200 DSP, 930 K logic cells and over 60 Mb of internal memory (including 22.5 Mb of UltraRAM). The chip also includes a soft-decision FEC block supporting low-density parity check (LDPC) decode/encode and Turbo decode for use in 5G wireless, backhaul, DOCSIS, and LTE applications.

The Module has on board 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.

# Block Diagram

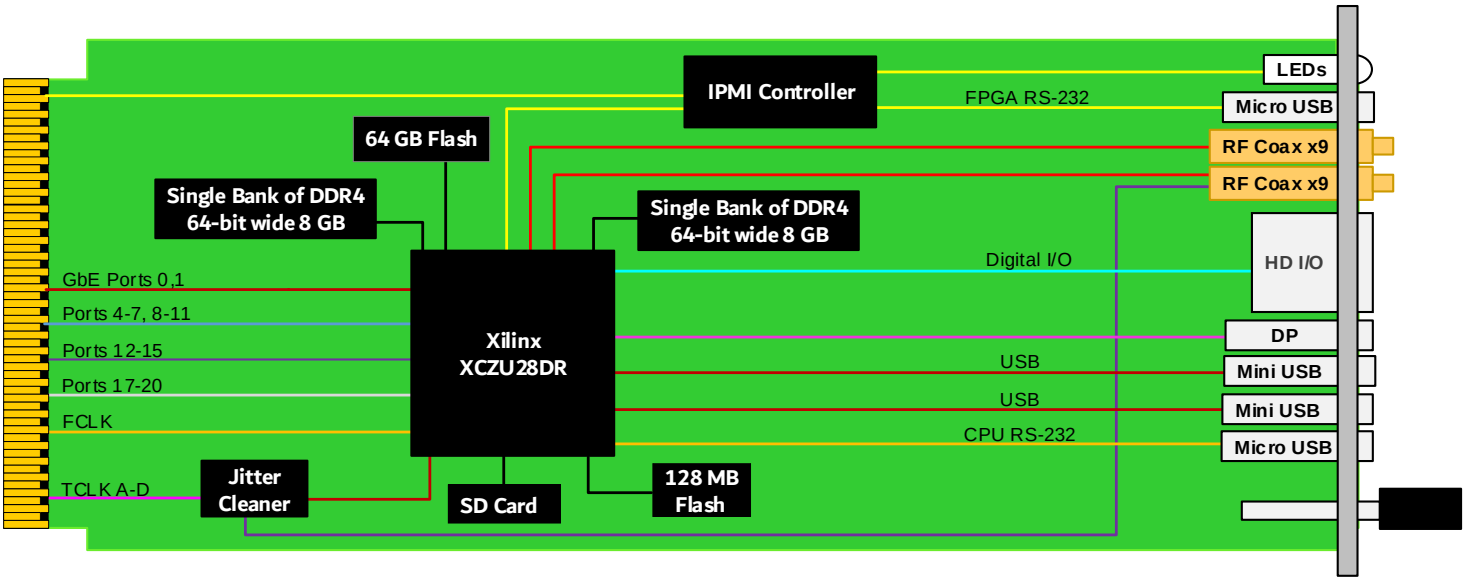



*Figure 1: AMC573 Functional Block Diagram*

# Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

# Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

# Specifications

| | | |
|---|---|---|
| **Architecture** | | |
| **Physical** | **Dimensions** | Double module, mid-size (full-size optional) |
| | | Width: 2.89” (73.5 mm) |
| | | Depth 7.11” (180.6 mm) |
| **Type** | **AMC FPGA Carrier** | Xilinx Zynq UltraScale+ RFSoC |
| **Standards** | | |
| **AMC** | **Type** | AMC.0, AMC.1, AMC.2, AMC.3 and AMC.4 |
| **Module Management** | **IPMI** | IPMI v2.0 |
| **GbE** | **Lanes** | Port 0 and 1 |
| **PCIe** | **Lanes** | x4 (4-7/8-11) or x8 (4-11) and additional ports on 12-15 and 17-20 |
| **10GbE/40GbE/SRIO** | | 4-7, 8-11 and additional ports on 12-15 and 17-20 |
| **Configuration** | | |
| **Power** | **AMC573** | TBD |
| | **RTM** | None |
| **Environmental** | **Temperature** | See ordering options |
| | | Storage Temperature: –40° to +85°C |
| | **Vibration** | Operating 9.8 m/s$^2$ (1G), 5 to 500 Hz on each axis |
| | **Shock** | Operating 30G on each axis |
| | **Relative Humidity** | 5 to 95% non-condensing |
| **Front Panel** | **Interface Connectors** | High-density multi-way RF Coaxial connectors x2 |
| | | Micro USB for RS-232 (management and CPU) |
| | | Dual Mini USB for USB |
| | | Display Port |
| | | High Density I/O Connector (4x RS-422 Input, 4x RS-422 Output, 8x SE +3.3 V Input, 8x SE +3.3 V Output) |
| | **LEDs** | IPMI management control |
| | | Debug (user defined) LED |
| | **Mechanical** | Hot swap ejector handle |
| **Software Support** | **Operating System** | Linux |
| **Other** | | |
| **MTBF** | MIL Hand book 217-F@ TBD hrs | |
| **Certifications** | Designed to meet FCC, CE and UL certifications, where applicable | |
| **Standards** | VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards | |
| **Warranty** | Two (2) years | |

**INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS**

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

### AMC573 – ABC-DEF-G0J

| A = Ports 12-15 to FPGA | D = SD Card | G = Clock Holdover Stability |
|---|---|---|
| 0 = Not routed<br>1 = Routed as SERDES* | 0 = No SD Card<br>1 = SD Card (32 GB) | 0 = Standard (XO)<br>1 = Stratum-3 (TCXO) |
| **B = Ports 17-20 to FPGA** | **E = FPGA Speed** | |
| 0 = Not routed<br>1 = Routed as SERDES* | 1 = Low<br>2 = High<br>3 = Reserved | |
| **C = Front Panel** | **F = PCIe Fabric** | **J = Temperature Range and Coating** |
| 1 = Reserved<br>2 = Mid-size<br>3 = Full-size<br>4 = Reserved<br>5 = Mid-size, MTCA.1 (captive screw)<br>6 = Full-size, MTCA.1 (captive screw) | 0 = No PCIe<br>1 = PCIe on ports 4-7<br>2 = PCIe on ports 8-11<br>3 = PCIe on ports 4-11 | 0 = Commercial (–5° to +55°C), No coating<br>1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane<br>2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic<br>3 = Industrial (–20° to +70°C), No coating<br>4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane<br>5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic<br>6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane**<br>7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic** |

Notes: *These ports are not LVDS compatible.
**Conduction cooled, temperature is at edge of module. Consult factory for availability.

# Related Products

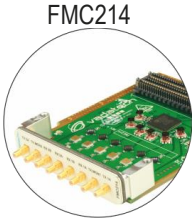
VT951

- MicroTCA rugged 1U 19” rackmount chassis platform
- Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration
- Supports up to six single module mid-size

AMC592

- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series™ data acquisition software

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD)

# Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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