AMC587

Dual ADC @ 6.4 GSPS and Dual DAC @ 12 GSPS, UltraScale+, AMC

AMC587

Key Features

- Xilinx UltraScale+™ XCVU13P FPGA
- Dual ADC @ 6.4 GSPS 12-bits or quad ADC at 3.2 GSPS with TI ADC12DJ3200
- Option for ADC12DJ3200, ADC12DJ2700 or ADC12DJ1600
- Dual DAC (AD9162 or AD9164) @ 12 GSPS, 16-bits
- Single bank of 64-bit wide DDR-4, 8 GB
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (protocols such as PCIe, SRIO, 1/10/40GbE, etc. are FPGA programmable)
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- Clock jitter cleaner
- IPMI 2.0 compliant

Benefits

- Closely coupled ADC and DAC for low-latency response, dual channel for I/Q
- Sampling rate >6 GSPS for radar and EW applications
- Xilinx UltraScale+™ XCVU13P FPGA provides powerful compute resource
- 8 GB of DDR-4 memory for high-bandwidth storage
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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The AMC587 provides dual-channel ADC with sample rates of up to 6.4 GSPS (TI ADC12DJ3200, ADC12DJ2700, or ADC12DJ1600) at 12-bits (or quad inputs at 3.2 GSPS) and a dual DAC (Analog Devices AD9162 or AD9164) update rate of up to 12 GSPS and direct RF synthesis at 6 GSPS at 16-bits making it suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.

The unit has an on-board, re-configurable UltraScale+™ XCVU13P FPGA which interfaces directly to ADC/DAC. The FPGA has interface to a single bank of DDR4 memory. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

Figure 1: AMC587

Block Diagram

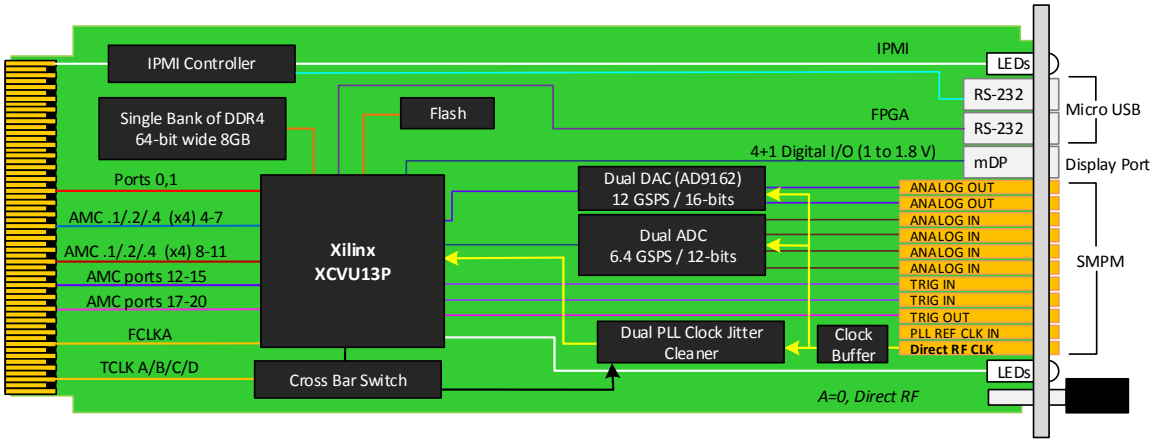

Figure 2: AMC587 Functional Block Diagram for Option A = 0

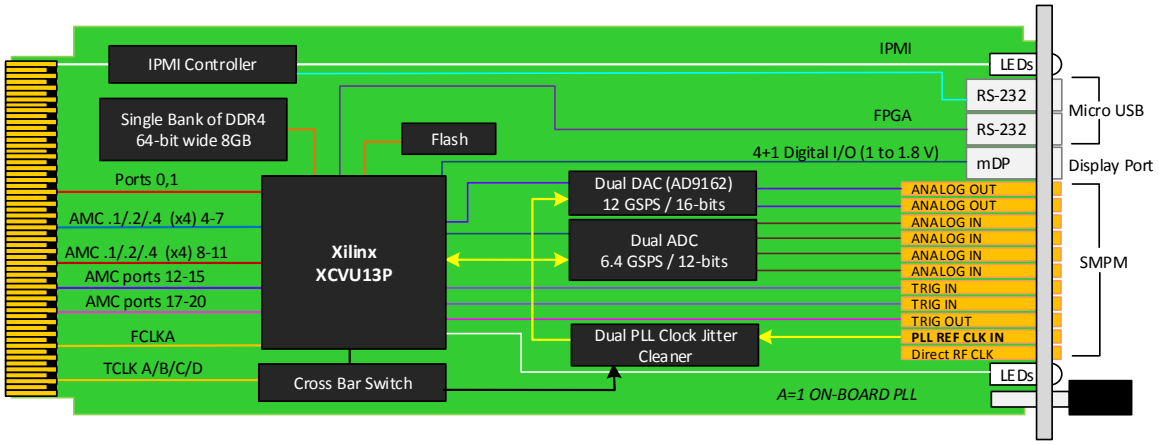

Figure 3: AMC587 Functional Block Diagram for Option A = 1

Notes:

- Direct RF CLK input is used when selecting ordering option A=0, for up to 8 GHz external clock directly routed to ADCs and DACs
- REF CLK IN is used when selecting ordering option A=1, for up to 500 MHz external clock routed through internal Clock Jitter cleaner, PLL and FPGA to the ADCs and DACs
- Each ADC has two SMPM inputs providing a total of 4 single ended analog inputs, the AMC587 can be used as dual ADCs at 6.4 GSPS or quad ADCs at 3.2 GSPS

Front Panel

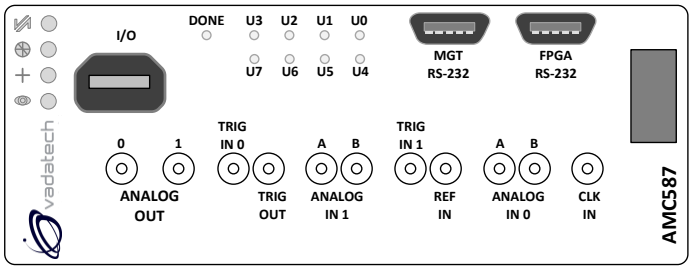

Figure 4: AMC587 Front Panel

Note: Front panel overlay labels are provided for information purpose only, the label text may be different on the actual product

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	Single module, full-size, (8 HP optional)
		Width: 2.89” (73.5 mm)
		Depth: 7.11” (180.6 mm)
Type	**AMC FPGA ADC/DAC**	Xilinx UltraScale™ XCVU13P FPGA
		Single bank of DDR4
		Dual ADC/Dual DAC
Standards		
AMC	**Type**	AMC.1, AMC.2 and AMC.4 (FPGA Programmable)
Module Management	**IPMI**	IPMI v2.0
PCIe	**Lanes**	Dual x4 via FPGA to AMC
SRIO/XAUI	**Lanes**	Dual x4 via FPGA to AMC
Ethernet	**GbE and 10 GbE**	Dual GbE and 10/40 GbE
Configuration		
Power	**AMC587**	~55 W application dependent (may go up to 75 W)
Environmental	**Temperature**	See ordering options and environmental spec sheet
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5-500 Hz on each axis
	Shock	Operating 30Gs each axis
	Relative Humidity	5 to 95% non-condensing
Front Panel	**Interface Connectors**	11x SMPM
		Micro USBs for MGT RS-232 and FPGA RS-232
		Mini DisplayPort for front panel I/O
	LEDs	IPMI management control
		8 user defined LEDs and 1 Status
	Mechanical	Hot swap ejector handle
Software Support	**Operating System**	Agnostic
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC587 – ABC-DEF-G0J

A = RF Direct Clock Sampling	D = ADC	G = Clock Holdover Stability
0 = Direct RF Clock 1 = On Board wide band PLL	0 = ADC12DJ3200 1 = ADC12DJ2700 2 = ADC12DJ1600	0 = Standard (XO) 1 = Stratum-3 (TCXO)
B = DAC	**E = FPGA Speed**	
0 = AD9162 1 = AD9164	1 = High (-2)** 2 = High (-2LE) 3 = Highest (-3E)**	
C = Front Panel Size	**F = PCIe Option**	**J = Temperature Range and Coating**
1 = Reserved 2 = Reserved 3 = Reserved 4 = 6 HP 5 = 6 HP, MTCA.1 (captive screw both side) 6 = Reserved 7 = 8 HP 8 = 8 HP, MTCA.1 (captive screw both side) 9 = 8HP, SLF*** (captive screw one side)	0 = No PCIe 1 = PCIe on ports 4 – 7 2 = PCIe on ports 8 – 11 3 = PCIe on ports 4 – 11	0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane* 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic*

Notes: *Conduction cooled, temperature is at edge of module
**Minimum Order Quantity applies for these FPGA SKU's.
***Single Latch Flange (SLF)

Related Products

VT951

- MicroTCA rugged 1U 19" rackmount chassis platform
- Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration
- Designed to meet MIL-STD-461E for EMI

FMC223

- Single module AD9739 DAC 14-bit at 2.5 GSPS
- 2 Vpp differential Analog output swing
- Programmable DSP clock

AMC726

- Intel® 4th Gen Core i7-4700EQ with QM87 chipset
- PCIe Gen3 x4 on ports 4-7 and 8-11 or single PCIe x8 on ports 4-11 (AMC.1)
- Serial over LAN

Contact

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