MPM_VPX570
Development Accelerator “Multi-Path Modulation” Software Package

Key Features
- Loopback pipeline ADC-DAC
- Quadrature Generator
- Multi-Path with N independent branches
- N independent variable delays and gain
- N independent Phase and Amplitude modulators
- Combiner for N branches
- MATLAB® model included

Benefits
- Accelerated development
- Flexibility covers a maximum of application cases
- Reference design with VHDL source code included
- MATLAB model allows user to start development prior to hardware supply
- AS9100 and ISO9001 certified company
The MPM_VPX570 Multi-Path Modulator Software package from VadaTech provides additional FPGA image and source code for the VPX570, intended to accelerate the development of a customer's end application.

The standard VPX570 is delivered by default with a BSP reference design loaded that allows a customer to test all of the board hardware features and acts as a start point for custom code development. The additional Multi-Path Modulator Software is a separate package implementing a pipeline between the ADC and the DAC using a subset of the available hardware functions.

The loopback pipeline between the ADC and the DAC integrates the following features:

- Quadrature Generator: Hilbert Transform to generate the complex representation of the real-valued ADC output
- Splitter: Splits the Quadrature generator's complex output to N independent branches
- Delay: Delays the input signal by a variable delay value
- Phase and Amplitude Modulator: Modulates the complex signal by a complex exponential, and applies gain
- Combiner: Sum the N Phase and Amplitude Modulator outputs
- (Optional) Controller: AXI4-Lite control of the Delay, Phase and Amplitude modulator parameters

A Matlab® model of the loopback pipeline is provided. This model does the following:

- Bit/cycle accurate simulation of each block of the loopback pipeline
- Performance measurement and comparison with Matlab® floating point equivalent functions
- Test of loopback parameters (delay, frequency, phase, gain)
- Generation of input/output files, for Xilinx simulator

Please note that VadaTech does not provide licenses for MATLAB® or third-party tools and these will have to be purchased separately.

MPM_VPX570 license conditions restrict use to implementation on VadaTech hardware only.
Quadrature Generator

The Quadrature Generator transforms the real input signal to a complex output. To do so, a Hilbert transform is used, in order to remove the negative frequency component of the real input signal.

Delay

Each branch has its own independent delay block. Delay value can be updated at each clock cycle. The coarse delay blocks use FPGA UltraRAM memory. The minimum coarse delay is 6 clocks cycles (due to URAM minimum latency), and the maximum coarse delay depends on how many URAM are implemented. This can be modified based on the number of signal branches in the system.

Phase and Amplitude Modulator

Each branch has its own modulator. The DDS Frequency/Phase as well as the gain can be updated at each clock cycle. The complete modulator pipeline operates in full precision. The input parameters DDS Frequency (phase increment) and DDS Phase (phase offset) are the inputs to a 32-bit Phase Accumulator, followed by a Phase Offset adder. The final phase is used as an address for a -SINE/COSINE lookup table. DDS Frequency and DDS Phase parameters can be changed every clock cycle to create a complex DDS output waveform.

Combiner

The combiner sums the N branch modulator outputs (48 bits), and rounds/saturates the sum output to 16-bit. The combiner output error, due to the quantization of the full scale 48-bit input to 16-bit output, stays below 0.5 LSB.

Optional AXI4-Lite Controller

For each branch, the Delay and the Phase and Amplitude Modulator have the following control signals:

- Delay Coarse
- Delay Fine
- DDS Frequency
- DDS Phase
- Gain

These control signals can be directly controlled by the user application, or routed to an AXI4-Lite Controller to control it via Microblaze, PCIe, etc.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay coarse</td>
<td>6</td>
<td>32768 (typical)</td>
<td>ADC sampling clock/16</td>
</tr>
<tr>
<td>Delay fine</td>
<td>0</td>
<td>15</td>
<td>ADC sampling clock</td>
</tr>
<tr>
<td>DDS frequency</td>
<td>0</td>
<td>4294967295</td>
<td>0-360°</td>
</tr>
<tr>
<td>DDS phase</td>
<td>0</td>
<td>4294967295</td>
<td>0-360°</td>
</tr>
<tr>
<td>Gain</td>
<td>0</td>
<td>8191</td>
<td>UFix13_12</td>
</tr>
</tbody>
</table>

Table 1: Loop Parameters Range

Matlab® Model

A Matlab model of the loopback pipeline is provided. This model does the following:

- Bit/cycle accurate simulation of each block of the loopback pipeline
- Performance measurement and comparison with Matlab floating point equivalent functions
- Test of Loopback parameters (delay, frequency, phase, gain)
- Generation of input/output files, for Xilinx simulator
Block Diagram

Figure 2: Multipath Modulator Signal Processing pipeline

Commands

VPX570 Tool v0.1
Usage: <cmd> [-<opts>]

HARDWARE CONTROL

i - Initialize the card
  3G Hz sampling clock from front panel CLK
  ADC and DAC both @3GSPS

dac_mode rpb rpw
  - Set DAC analog parameters
    mode: nrz, mrb, tzc, rf
    rpb: rpb0, rpb1, rpb2, rpb3, rpb4
    rpw: rpw0, rpw1, rpw2, rpw3, rpw4

status
  - Set DAC internal gain (0 to 1023, default 512)
  - Get ADC/DAC sync status

LOOPBACK CONTROL

set_loop idx dl_coarse dl_fine ph freq gain
  - Set loopback parameters
    idx: sub range index (1 to number of subrange)
    dl_coarse: sub range delay, from 0 to 32767 (unit 167 MHz period)
    dl_fine: sub range delay, from 0 to 15 (unit 30 MHz period)
    ph: sub range modulator phase, from 0 to 360 deg
    freq: sub range modulator frequency (unit Hz)
    gain: sub range gain, from 0 to 4095 (4095 dB gain)

get_loop
  - Get loopback parameters

adc_source source
  - Set ADC output: 0= ADC samples, 1= fixed Fs/4 sine wave, 2=zeros

DEBUG COMMAND

d <gp>
  - Dump FPGA register contents

w <addr> <val>
  - Write value at FPGA address

r <addr>
  - Read back at FPGA address

x= <addr>
  - Dump device's register contents

rd <addr> <addr> <val>
  - Write value to the device's address

sa <cpl> <addr>
  - Read value from the device's address

Device Key:

g = GPSP
a = EV12AS350A
b = EV12DS408AZP
c = Altim PE43712 for front panel CLK port
r = Altim PE43712 for front panel REF CLK port

Figure 3: Console Command Tool
Related Products

- **VPX004**
  - Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
  - Automatic fail-over with redundant VPX004
  - 1GbE base switch with dual 100/1000/10G uplink

- **VPX570**
  - 3U ADC 12-bit @ 5.4 GSPS and DAC 12-bit @ 6 GSPS, Virtex UltraScale+
  - PCIe Gen3 x 16 (or x8 or x4) or No-PCIe SERDES option (SRIIO, XAUI, Aurora)
  - Direct RF clock or on-board PLL option

- **VTX870**
  - Open VPX benchtop development platform
  - Dedicated Switch/management slot
  - Up to five 3U VPX payload slots