

VPX514

FPGA Carrier with FMC Interface, 6U VPX



VPX514

Key Features

- VPX (VITA 46) FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 57
- VPX514 only takes power from the VPX chassis (there are no other interfaces going to the back plane)
- Dual 10GbE via SFP+ interfaces
- Xilinx Virtex-6® FPGA in FF1759 package
- On board PLL for buffering/multiplying and jitter cleaner
- On board Freescale QorIQ PPC1020 with DDR3

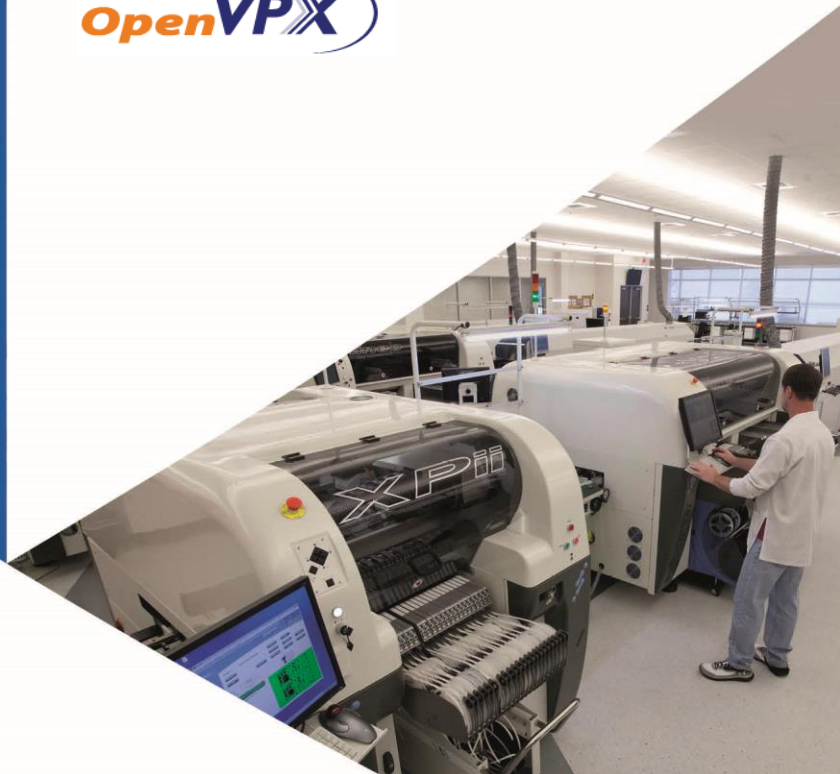
Benefits

- Option for up to 4 GB of DDR3 memory
- Reference design with VHDL source code speeds application development
- Design utilizes proven VadaTech subcomponents and engineering techniques
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™



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VPX514

The VPX514 is an VPX FPGA Carrier with an FMC (VITA 57) interface. The VPX514 is compliant to the VPX VITA 46 specification. The FPGA has an interface to four banks of DDR3 memory (32-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The VPX514 has a single FMC connector per VITA 57. This allows having a single Carrier with multiple-different FMC modules in the system.

The on board PPC can run at 800 MHz with 512 MB of DDR3, 8 MB of boot flash and 128 MB of user Flash. The PPC has an x4 PCIe interface to the FPGA in addition to its local bus. The PPC has its dual GbE routed to ports 0 and 1 of the VPX.



Figure 1: VPX514

Block Diagram

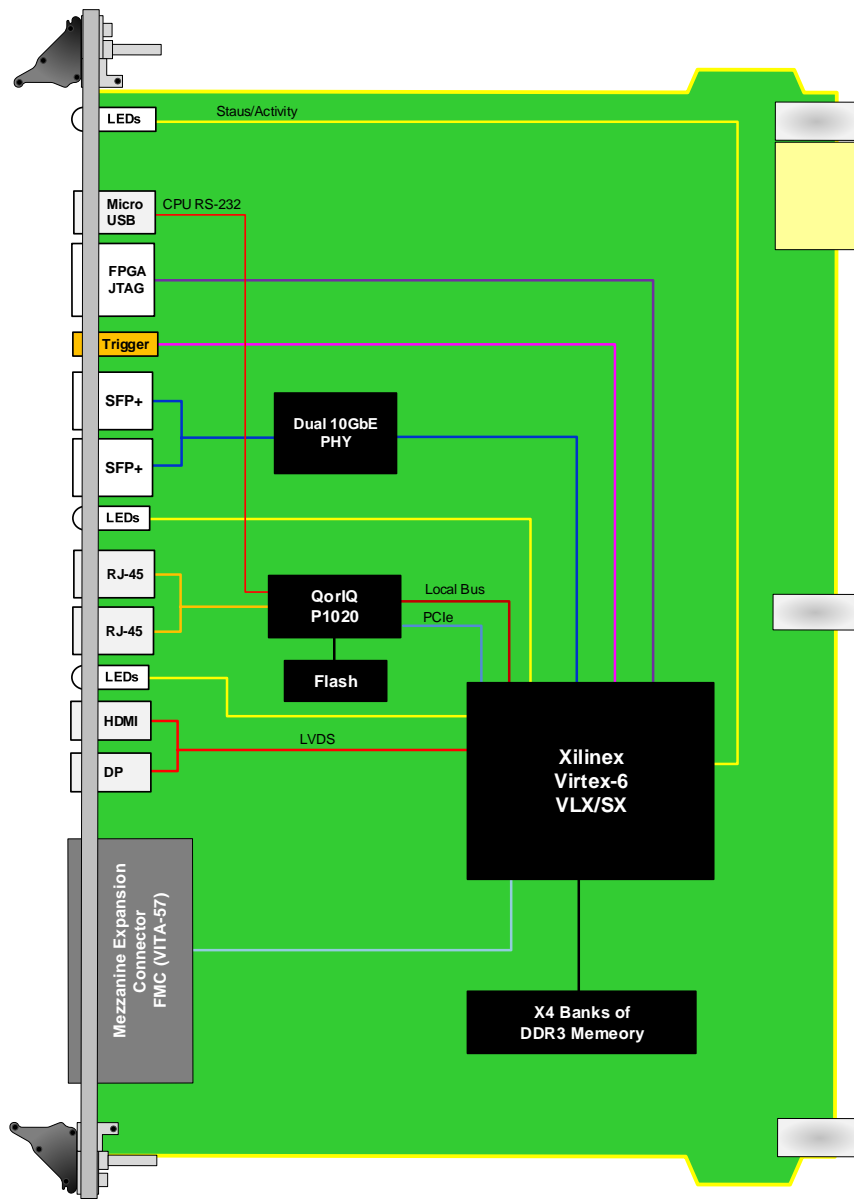


Figure 2: VPX514 Functional Block Diagram

Front Panel

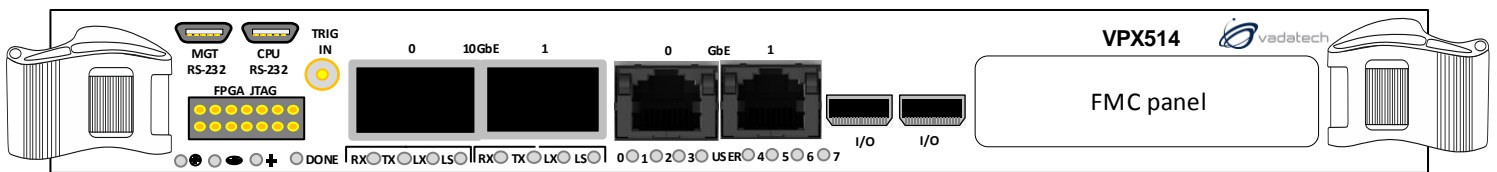


Figure 3: VPX514 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

Specifications

Architecture	
Physical	Dimensions 6U, 1" pitch
Type	FPGA Xilinx Virtex-6®
	Memory x4 Banks DDR3
	Single FMC slot
Standards	
VPX	Type VITA 46 (FPGA Programmable)
Configuration	
Power	VPX514 ~40 W (without Mezzanine)
Front Panel	JTAG Standard JTAG header
	Micro USB RS-232 from FPGA
	Trigger Trigger/In to FPGA
	1/10GbE Dual SFP+
	RJ-45 X2 GbE
	HDMI LVDS to FPGA
	DP LVDS to FPGA
	LEDs X8 User defined from FPGA
	GbE/10GbE Link/Activity
VPX Interfaces	Slot Profiles See ordering options
Software	Operating System Linux, Windows, Solaris and VxWorks
Other	
MTBF	MIL Hand book 217-F@ TBD hrs
Certifications	Designed to meet FCC, CE and UL certifications, where applicable
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards
Warranty	Two (2) years

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX514 – AB0-DE0-0HJ

A = DDR3 Memory	D = FPGA	
1 = No Memory 2 = 512 MB per bank (2 GB total) 3 = 1 GB per bank (4 GB total)	1 = Reserved 2 = Reserved 3 = Reserved 4 = XC6VLX240T 5 = XC6VLX365T 6 = XC6VLX550T 7 = XC6VSX475T 8 = Reserved	
B = SFP+ TXCVR for 1/10GbE Fabric	E = FPGA Speed	H = Environmental
0 = No SFP+ TXCVR 1 = 10GBase SR 2 = Reserved 3 = 10GBase LR 4 = 1G LC/SX (850nm) 5 = 1G LC/LX (1310nm) 6 = Copper 1000 Mbit 7 = Reserved	1 = Low 2 = High	See Environmental Specification Table below
		J = Conformal Coating
		0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

Option H	Air Cooled		Conduction Cooled		
	H = 0	H = 1	H = 2	H = 3	H = 4
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4)

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