VPX588

Quad ADC @ 3 GSPS with Quad DAC @ 12 GSPS, Virtex UltraScale+™, 3U VPX

VPX588

Key Features

- Xilinx Virtex UltraScale+™ XCVU13P FPGA
- Quad ADC 14-bit @ 3 GSPS (AD9208)
- Quad DAC 16-bit @ 12 GSPS (AD9162 or AD9164)
- Single bank of DDR4 64-bit wide 8 GB Total
- 16 SERDES as PCIe/SRIO/10GbE/40GbE/Aurora to P1
- 8 SERDES as PCIe/SRIO/10GbE/40GbE/Aurora to P2
- Clock Jitter cleaner
- Option for Direct RF Clock sampling for the ADC/DAC
- Health Management through dedicated Processor

Benefits

- Closely coupled ADC and DAC for low-latency response, dual channel for I/Q
- Sampling rate >6 GSPS for radar and EW applications
- Xilinx UltraScale+™ XCVU13P FPGA provides powerful compute resource
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX588

The VPX588 provides quad ADC sampling rates of up to 3 GSPS at a 14-bit resolution (AD9208). Also, quad DAC delivers update rates of up to 12 GSPS and incorporates direct RF synthesis capable of 6 GSPS at a 16-bit resolution (Analog Devices AD9162 or AD9164). This makes VPX588 suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.

The unit has an onboard, re-configurable Virtex UltraScale+™ XCVU13P FPGA that directly interfaces with ADC/DAC and a single bank of DDR4 memory channels (64-bit wide for a total of 8 GB). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.
The module routes x16 SERDES to P1 which can run any protocol (i.e PCIe/SRIO/10G/40G/Aurora) and x8 SERDES with 16 LVDS signals to P2.

The VPX588 10 HP panel size occupies two slots in a chassis and is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

Figure 1: VPX588

Block Diagram

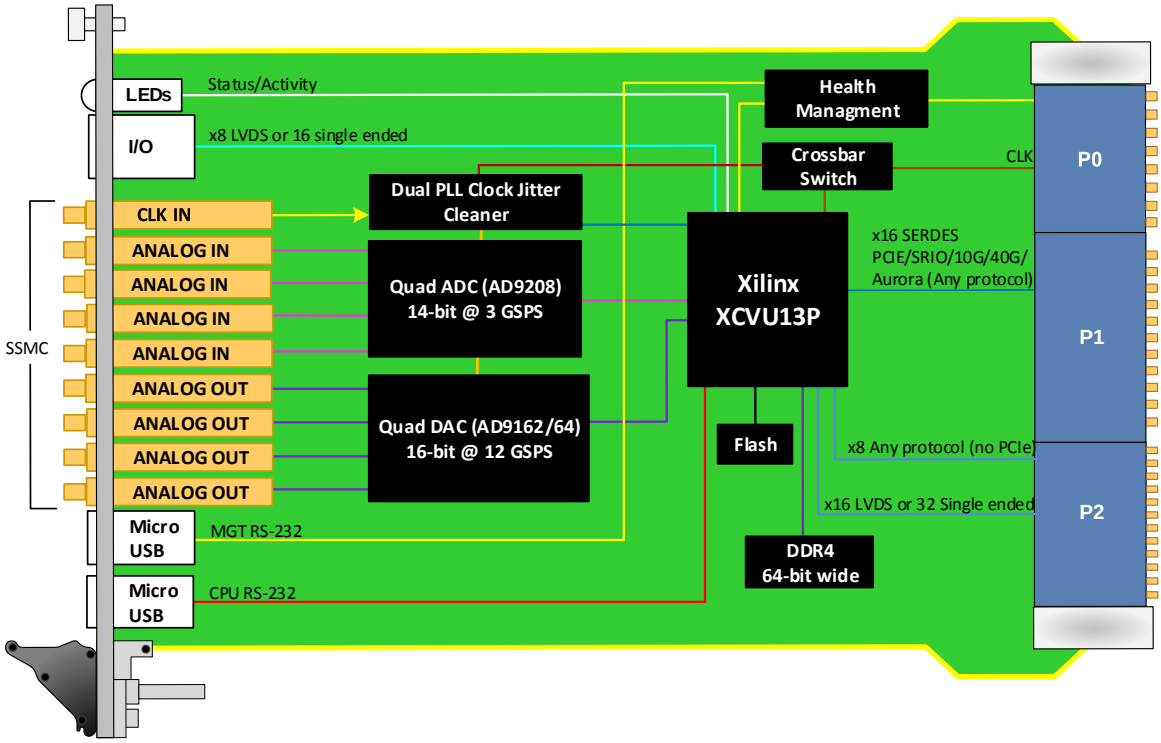

Figure 2: VPX588 Functional Block Diagram for Onboard Wideband PLL A = 1

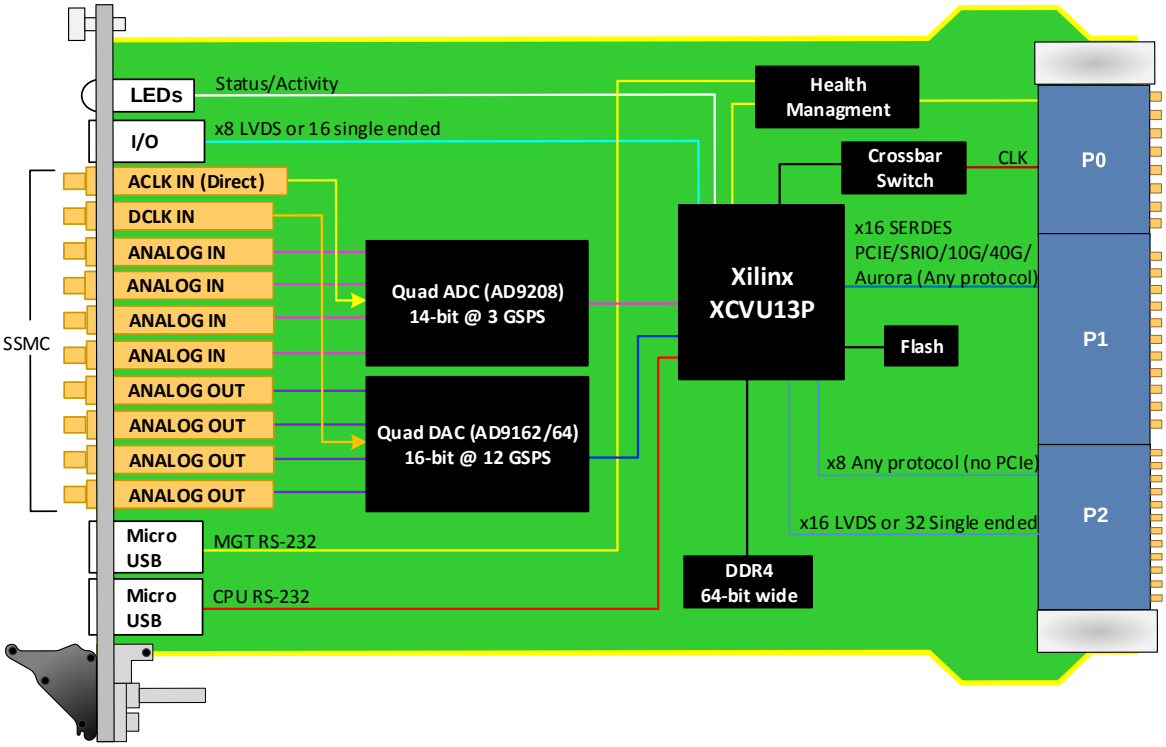

Figure 3: VPX588 Functional Block Diagram for Direct RF A = 0

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as VPX modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Data Acquisition

VadaTech offers a wide range of FPGA VPXs, RTMs, FMC Carriers and FMCs that can be combined to build a Data Acquisition (DAQ) sub-system. The DAQ Series software, when used with a supported hardware configuration, provides all that is needed to configure the system, acquire data and transfer it to a host processor. It also includes a user-configurable Graphical User Interface (Figure 4), which incorporates real-time display of acquired data. The host can be within the MTCA system or, via PCI113 or PCI123, in a separate PC. Full documentation is provided to allow users to customize system behavior or develop their own application on the VPX/FMC hardware.

The DAQ includes data acquisition software that allows users to get up and running quickly and easily, while providing a high level of performance and allowing the user to extend functionality by adding their own FPGA code. Please contact VadaTech sales for the latest information on supported combinations of VadaTech hardware. (Note that the DAQ Series software is not currently supported for 3rd party hardware).

Components provided in the DAQ software include:

- System libraries to configure clocking and triggers
- Sequencer to configure the acquisition (duration, start, stop)
- High-performance DMA firmware for acquiring ADC outputs and transferring to host processor
- Linux driver for host processor (e.g. VPX75x)
- EPICS channel access client API
- Pre-configured GUI (based on Qt Creator)

This software set allows the user to acquire, transfer and display data without the need for any user programming of the hardware. Status information is included in the GUI display, to ease integration and debugging activity.

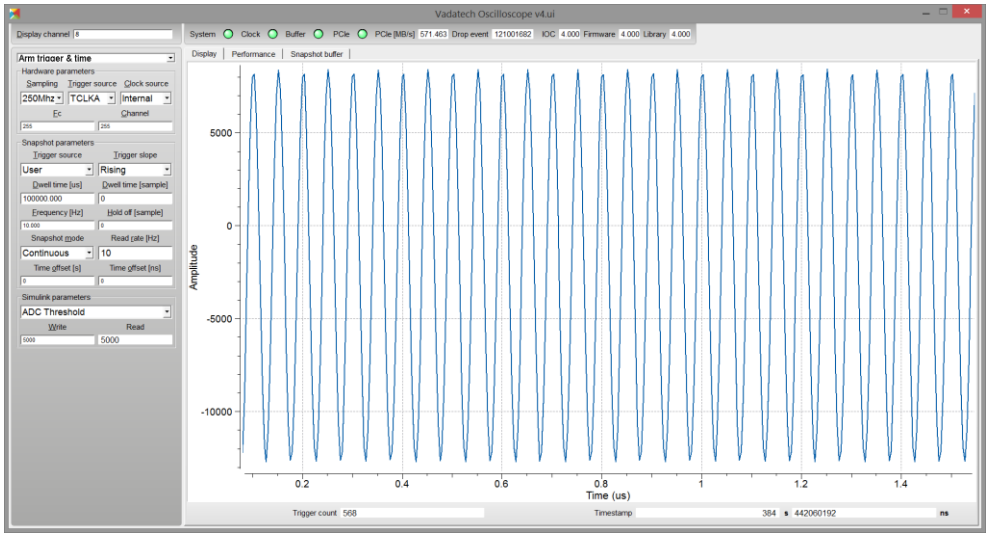

Figure 4: Typical Graphic User Interface Display

The data acquisition software provided as part of the DAQ can be used as-delivered without the user needing to develop any FPGA code.

Full source code is provided for the libraries, sequencer, DMA, Linux driver and GUI, allowing users to easily customize or brand to their own requirements at the exception of a low level PCIe IP from Xilinx provided only as Netlist (this low-level block doesn't require modification/customization from integrators or end-users).

Specifications

Architecture		
Physical	**Dimensions**	3U, 10 HP
FPGA		Xilinx UltraScale+™ XCVU13P FPGA
Configuration		
Power	**VPX588**	65W (FPGA load dependent)
Front Panel	**SMPM**	10x SMPM
	Micro USB	RS-232 from Health Management CPU
		RS-232 from FPGA
	LEDs	8 User defined/Activity and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	x16 SERDES could be configured as PCIe/SRIO/10GbE/40GbE/Aurora on P1
		x8 SERDES could be configured as SRIO/10GbE/40GbE/Aurora on P2
		x16 LVDS or 32 single-ended on P2
		RTM management on P1/P2
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX588 – ABC-DEF-GHJ-KL0

A = RF Direct Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles	K = Nyquist Zones (ADC ONLY)
0 = Direct RF Clock 1 = Onboard Wideband PLL	1 = High (-2)* 2 = High (-2LE) 3 = Highest (-3E)*	0 = 10 HP	0 = 1st/2nd Nyquist 1 = 2nd/3rd Nyquist
B = DAC	**E = Clock Holdover Stability**	**H = Environmental**	**L = VPX Connector Type**
0 = Quad DAC Channels (AD9162) 1 = Quad DAC Channels (AD9164) 2 = No DAC 3 = Octal DAC Channels (AD9162)+ 4 = Octal DAC Channels (AD9164)+ 5 = Quad DAC (AD9162) with attenuation+† 6 = Octal DAC (AD9162) with attenuation+†	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification	0 = Standard 50u Gold Rugged 1 = KVPX Connectors
C = ADC	**F = PCIe Option (P1)****	**J = Conformal Coating**	
0 = Quad ADC Channels (AD9208) 1 = Dual ADC Channels (AD9208) 2 = No ADC 3 = Octal ADC Channels (AD9208)++	0 = No PCIe (40GbE, 10GbE, SRIO, etc.) 1 = x4 or x8 PCIe via FPGA 2 = quad x4, or dual x8 via FPGA	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	

Notes: *Minimum Order Quantity applies for these FPGA SKU's.

**When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

+Option C must be 2 (C = 2) to select this option, Minimum Order Quantity applies.

++Option B must be 2 (B = 2) to select this option, Minimum Order Quantity applies.

†Attenuators are programmable

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Available Signal Bandwidth

Ordering Option (Number of Channels)	Interpolation (Minimum)	Maximum Fdata (MHz)	Available Signal Bandwidth (MHz)
Dual/Octal/Quad ADC (C = 0/1/3)	Bypass x1	3000	1500
Quad DAC (B = 0/1)	Bypass x1	Fdac = 5000	Fdac/2 = 2500
Octal DAC (B = 4)	Decimation x4	Fdac/4 = 1250	80% to 90% of 1250 (total I/Q)

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX517

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex-7 410T FPGA in FFG-900 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

Contact

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